REMARKS

The Official Action mailed June 26, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to October 26, 2002. Accordingly, Applicants respectfully submit that this response is being timely filed.

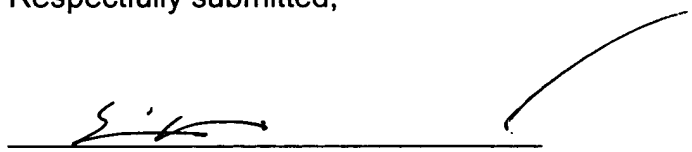
Applicants note with appreciation the consideration of the Information Disclosure Statements filed on June 2, 1999; March 31, 2000; June 21, 2000; July 30, 2001; February 15, 2002; and April 18, 2002. A further IDS is submitted herewith and careful review and consideration of this IDS is requested.

Claims 1-76 are pending in the present application, of which claims 1, 10, 19, 32, 45 and 68 are independent. All independent claims have been amended herewith and for the reasons set forth in detail below, these claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action rejects claims 1-76 as anticipated by JP 02-234134 to Sumiyoshi et al. In response, Applicants have amended the independent claims to recite that a semiconductor layer of a TFT has substantially no grain boundaries (see, page 14, last paragraph to page 15 of the specification). Sumiyoshi does not teach or suggest all the elements of the independent claims, as amended, either explicitly or inherently. The polycrystalline semiconductor films disclosed in Sumiyoshi include grain boundaries which provide barriers against carrier transportation and are different from the semiconductor layer of the present invention. Accordingly, reconsideration and withdrawal of the rejection of claims 1-76 under 35 U.S.C. § 102(e) is in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 10, 19, 32, 45 and 68 as follows:

1. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least one thin film transistor formed on said insulating surface, said thin film transistor having a [polycrystalline] semiconductor layer comprising source, drain and channel regions;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over said [interlayer] insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

wherein said [polycrystalline] semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction,

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.

10. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least one thin film transistor formed on said insulating surface, said thin film transistor having a [polycrystalline] semiconductor layer comprising source, drain and channel regions;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over said [interlayer] insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

wherein said [polycrystalline] semiconductor layer exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction, and

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.

19. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a [polycrystalline] semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said [interlayer] insulating film;

wherein said [polycrystalline] semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction,

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.

32. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a [polycrystalline] semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said thin film transistor and said [interlayer] insulating film;

wherein said [polycrystalline] semiconductor layer comprises silicon and exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction, and

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.

45. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least an n-channel thin film transistor and at least a p-channel thin film transistor both formed over said [first] substrate, each of said n-channel and p-channel thin film transistors comprising:

a [polycrystalline] semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said [interlayer] insulating film;

wherein said [polycrystalline] semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction, and

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.

68. (Amended) A semiconductor device comprising:

a [first] substrate having an insulating surface;

[a second substrate opposing said first substrate;]

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a [polycrystalline] semiconductor layer having source, drain and channel regions;

an [interlayer] insulating film comprising an inorganic material formed on said thin film transistor; [and]

an organic resin film provided over said [interlayer] insulating film; and

a pixel electrode provided over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film;

wherein said [polycrystalline] semiconductor layer exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction, and

wherein said [polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer] semiconductor layer has substantially no grain boundaries.